REPORT : RECEIVING AND TRANSMITTING THE DATA USING MEMORY AS AN INTERMEDIATE

**Components used:**

1. *Receiver:*

The working of the receiver is same as in the previous assignment (with rx\_data as the array of bits which the receiver gives memory as input) except for the two new logics introduced in the code namely:

* **Rx\_full** = rx\_full states that all the bits have been read by the receiver, hence after reading all the 8 bits the receiver gives its value as 1 i.e., we get this value in the start and the idle state.
* **Reset=** when reset is 1 , the clock starts its counting from 0 and when it is one means receiver has done its work, hence it gives rx\_full = 1 as well.

1. *Transmitter:*

The working of the transmitter is same as in the previous assignment (with tx\_data as the array of bits which the memory gives it as input) except for the two new logics introduced in the code namely:

* **Tx\_empty =** tx\_empty states that all the bits have been transmitted by the transmitter, hence after transmitting all the 8 bits the transmitter gives its value as 1 i.e., we get this value in the idle state.
* **Reset=** when reset is 1 , the clock starts its counting from 0 and when it is one means receiver has done its work, hence it gives tx\_empty= 1 as well.

1. *Memory:*

When the receiver gives its output as input to the memory component of the circuit then it stores it in an array of size 256 where each block stores a bit vector received from the receiver, then memory gives this stored bit vector to the transmitter as input.

The code of this component consists of:

Reset: It starts the counting of clock from 0.

enb: When it is 1, the memory transmits data to the transmitter.

Wea: When it is 1 , the memory receives data from the receiver.

Addra: same as wr\_addr

Addrb: same as rd\_addr

Dina: input of memory and output of receiver.

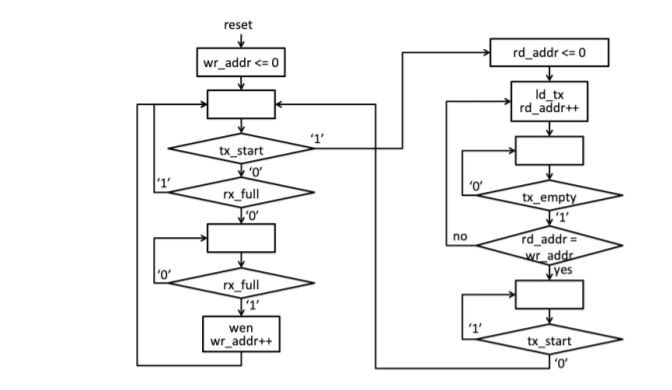
Doutb: output of memory and input of transmitter.

1. ***Timing circuit:***

The timing circuit synchronises the working of all these 3 components. In the working all this circuit , 9 states are involved ( s1 to s8 and an extra state to synchronise the clock of the receiver and the transmitter) , timing circuit decides the present state according to the code written.

The components of this are:

* wen : When it is 1, then it gives signal to the memory to receive input from the receiver.
* wr\_addr : It is a binary counter which counts whenever we give a byte input to receiver, then wr\_addr increases itself by one and gives signal to memory to store the output of the receiver.
* rd\_addr : Same as wr\_addr, it is also a binary counter which counts whenever, the transmitter is empty, and tx\_start is one, it increases itself by one and gives a byte to the transmitter.
* ld\_tx : It becomes one whenever we need to turn on the transistor.
* txclk : It is a normal clock of 200MHz.
* reset : it gives zero value to all signals and outputs and restart the whole system.
* tx\_start : a manual input which enables transmitting.
* rx\_full: it turns to 1 when a complete byte is received.
* tx\_empty : it turns to 1 whenver transmitter transmits a byte and ready for the next byte.



***Thanks***

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